FUSE CIRCUIT AND SEMICONDUCTOR DEVICE INCLUDING THE SAME

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TECHNICAL FIELD OF THE INVENTION

The present invention relates to a semiconductor device having a fuse circuit therein.

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BACKGROUND OF THE INVENTION

A conventional fuse circuit formed in a semiconductor device includes a conductive line and a pair of electrodes, connected to the ends of the conductive line. The conductive line includes a disconnection region, which is shaped to be narrower or thinner and is disconnected easily. The conductive line may be made of metal. In operation, a predetermined voltage is applied between the electrodes so that a predetermined current flows through the conductive line. When a specific amount of current flows through the conductive line, the disconnection region is melt and disconnected.

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According to the above described conventional fuse circuit, particles of the conductive line may be left over on the fuse circuit or on the semiconductor device. As a result, a reliability of the fuse circuit and the semiconductor device is decreased.

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OBJECTS OF THE INVENTION

Accordingly, it is an object of the present invention to provide a semiconductor device in which a reliability of a fuse circuit is improved.

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Additional objects, advantages and novel features of the present invention will be set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The objects and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

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SUMMARY OF THE INVENTION

According to the present invention, a semiconductor device includes a fuse circuit, which includes a first conductive region and a second conductive region. The first conductive region has a multi-layered structure, and the second conductive region has a less layered structure than the first conductive region.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating the whole image of a semiconductor device according to a first preferred embodiment of the present invention.

Fig. 2A is an enlarged plan view illustrating a fuse circuit according to the first preferred embodiment.

Fig. 2B is a cross-sectional view taken on line A-A' in Fig. 2A.

Fig. 3 is an explanatory diagram showing a specific design of the fuse circuit according to the first preferred embodiment.

Fig. 4 is an explanatory diagram showing an arrangement of fuse circuit according to the present invention.

Fig. 5 is an explanatory diagram showing an arrangement of fuse circuit according to a second preferred embodiment of the present invention.

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DETAILED DISCLOSURE OF THE INVENTION

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which forma part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These preferred embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other preferred embodiments may be utilized and that logical, mechanical and electrical changes may be

made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and scope of the present inventions is defined only by the appended claims.

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Fig. 1 is a block diagram illustrating the whole image of a semiconductor device according to a first preferred embodiment of the present invention. A semiconductor device 10 includes at least one fuse circuit 12 therein. The fuse circuit 12 may be a redundant fuse; a fuse used for adjusting a resistance and/or capacity; a fuse used for switching logic circuits in the semiconductor device 10; and a fuse used for adjusting an output level of signal. The present invention is applicable to a variety kinds of semiconductor devices.

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Fig. 2A is an enlarged plan view illustrating the fuse circuit 12 formed on a semiconductor substrate according to the first preferred embodiment. Fig. 2B is a cross-sectional view taken on line A-A' in Fig. 2A. The fuse circuit 12 includes a pair of electrode pads 14a and 14b; and a conductive line (16 & 18) connected between the electrode pads 14a and 14b. The conductive line (16 & 18) may be made of metal, such as Al and Cu, multicrystal silicon, and tungsten siliside (Wsix).

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From a plan view, the conductive line includes a first conductive region 16 and a second conductive region 18. On the

other hand, from layered structure of view (cross-sectional view), the conductive line (16 & 18) includes first to third conductive layers 24, 26 and 28, and a passivation layer 22, as shown in Fig. 2B. The passivation layer 22 is not formed over the second conductive region 18. In the first conductive region 16, through holes 20 are formed in interlayer insulating layers. The second conductive region 18 is formed on the upper most layer 28.

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The first conductive region 16 has a multi-layered structure, as shown in Fig. 2B, in order to reduce current density thereat. The second conductive region 18 has a single layer structure as shown in Fig. 2B, in order to increase current density thereat. The second conductive region 18 may have a multi-layered structure, but should be less layered than the first conductive region 16. For instance, the first conductive region 16 has more than four-layered structure and the second conductive region 18 has double-layered structure. According to the present invention, the second conductive region (disconnection region) 18 may be disconnected selectively and reliably, because electric current tends to be concentrated on the second conductive region 18. As a result, a fuse circuit can be designed small in size on a semiconductor substrate.

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Fig. 3 is an explanatory diagram showing a specific design of the fuse circuit 12. A length "L" of the second conductive region 18 is designed not to be larger than a double of a width "W" of the

conductive line (16) for better fabrication process. If the length "L" of the second conductive region 18 is longer than "2W", the selectivity of fuse disconnection would be decreased.

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Fig. 4 is an explanatory diagram showing an arrangement of fuse circuits according to the present invention. A plurality of conductive lines (16 + 18) are arranged in parallel to each other and the second conductive regions 18 are not located adjacent one another. In other words, the second conductive regions 18 are arranged alternately as shown in Fig. 4.

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In operation, when a predetermined voltage is applied between the electrode pads 14a and 14b, electric current flows through the conductive line (16 &18). When a predetermined amount of electric current through the second conductive region 18, the region 18 is melt and disconnected.

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Fig. 5 is an explanatory diagram showing an arrangement of fuse circuit according to a second preferred embodiment of the present invention. Fig. 5 corresponds to Fig 4. The fuse circuit is of a laser trimming type. In other words, a laser beam is applied to the second conductive region 18 in order to disconnect it. The other structure and operation is almost the same as the first preferred embodiment, and the same description is not repeated to avoid redundancy. According to the second preferred embodiment, shown in Fig. 5, the

second conductive regions 18 are arranged alternately, so that a laser beam can be applied to a specific region 18 reliably. In other words, unnecessary regions are prevented from being disconnected accidentally. As a result, the conductive lines can be arranged with a smaller pitch or distance.